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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,542	06/27/2003	Akihisa Shimomura	0756-7171	6138

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EXAMINER	
ISAAC, STANETTA D	
ART UNIT	**PAPER NUMBER**
2812	

DATE MAILED: 03/25/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/607,542	SHIMOMURA ET AL.	
	Examiner	Art Unit	
	Stanetta D. Isaac	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 December 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) *2,4,6,8,10,12,25 and 27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3,5,7,9,11,13-24,26 and 28-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 June 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

LYNNE A. GURLEY
PRIMARY PATENT EXAMINER
TC 2800, AU 2812

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *6/27/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to the election and amendment filed on 12/21/04. Currently, claims 1-37 are pending.

Election/Restrictions

Applicant's election without traverse of Species I (figures 7A-7E) in the reply filed on 12/21/04 is acknowledged.

Claims 2, 4, 6, 8, 10, 12, 25, and 27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Species II-IV, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 12/21/04.

Priority

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

The information disclosure statement (IDS) was submitted on 6/27/03. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Specification

The specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claim Objections

Claim 14 is objected to because of the following informalities: "...radiant heat method and gas heat method rapid thermal annealing." Should be "...radiant heat method, gas heat, method and rapid thermal annealing." Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 19 recites the limitation "introducing an impurity element into the crystalline semiconductor layer ..." in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1, 3, 5, 7, 9, 11, 13-24, 26, and 28-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Buynoski US Patent 6,376,336 in view of Hwang et al., US Patent 6,682,964.

Buynoski discloses the semiconductor method substantially as claimed. See figures 1-6, and corresponding text, where Buynoski shows, pertaining to claims 1 and 3, a method of manufacturing a semiconductor device, comprising: forming a crystalline semiconductor layer **16** by heating an amorphous semiconductor layer over a substrate **12** that has an insulating surface **14** (after adding a metal element for accelerating crystallization thereto, for claim 3; figure 1; 4, lines 40-47; col. 9, lines 43-50 for transitional metals, ***Note***: that the Examiner takes the position that a crystalline semiconductor layer is formed by heating an amorphous semiconductor layer after adding a metal element for accelerating crystallization, since the monocrystalline silicon film, taught by Buynoski, includes transitional metals that are conventionally used for crystallization); introducing an impurity of one conductivity type **18/20** into the crystalline semiconductor layer (figure 2; col. 5, lines 40-46); removing a surface portion of the crystalline semiconductor layer (figure 5; col. 10, lines 17-20); and forming a channel portion of an insulated gate field effect transistor form a remaining portion of the crystalline semiconductor layer (col. 13, lines 60-65, ***Note***: that the Examiner takes the position that forming a channel portion of an insulated gate field effect transistor from a remaining portion of the

crystalline semiconductor layer is performed since the SOI wafer, taught by Buynoski, may be further processed by methods known in the art for preparing a desired semiconductor device). In addition, Buynoski shows, pertaining to claims 9 and 11, a method of manufacturing a semiconductor device, wherein 40 nm or more of the thickness of the surface portion is removed (col. 13, lines 1-10 and 22-43). Also, Buynoski shows, pertaining to claims 24 and 26, a method of manufacturing a semiconductor device, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to $5 \times 10^{18}/cm^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 7, lines 35-42).

In addition Buynoski shows, pertaining to claims 13, 19 and 28, a method of manufacturing a semiconductor device, comprising: forming an amorphous semiconductor layer having a thickness of 60 nm or more (figure 1; 4, lines 40-47; col. 13, lines 1-10 and 22-43, ***Note***: that the Examiner takes the position that a amorphous semiconductor layer having a thickness of 60 nm or more is included); crystallizing the amorphous semiconductor layer to obtain a crystalline semiconductor layer (figure 1; 4, lines 40-47; col. 13, lines 1-10 and 22-43, ***Note***: that the Examiner takes the position that crystallizing the amorphous semiconductor layer to obtain a crystalline semiconductor layer is performed since a monocrystalline silicon film is, taught by Buynoski); introducing an impurity element **18/20** into the crystalline semiconductor layer by accelerating the impurity element with the acceleration voltage 30 kV or less (figure 2; col. 5, lines 40-46, ***Note***: that the Examiner takes the position that the acceleration voltage of 30 kV or less is incorporated since Buynoski teaches conventional ion implantation techniques); removing a surface portion of the crystalline semiconductor layer which is re-crystallized (crystalline semiconductor layer, for claim 19; figure 5; col. 8, lines 3-8 for heat treatment; col.

10, lines 17-20, ***Note***: that the Examiner takes the position that the surface of the crystalline semiconductor layer is re-crystallized since the semiconductor wafer, taught by Buynoski, is subjected to a heat treatment for the removal of the impurities within the monocrystalline silicon film). Also, Buynoski shows, pertaining to claim 14, a method of manufacturing a semiconductor device, wherein a method for crystallizing the amorphous semiconductor layer is selected from one of furnace annealing, radiant heat method, gas heat method, and rapid thermal annealing (col. 5, lines 27-39 ***Note***: that the Examiner takes the position that at least one of theses conventional heat treatments methods are performed). Buynoski shows, pertaining to claims 16, 21 and 31, a method of manufacturing a semiconductor device, wherein a thickness of the surface portion of the crystalline semiconductor layer removed is 10 nm to 50 nm (col. 13, lines 1-10 and 22-43). In addition, Buynoski shows, pertaining to claims 17, 22 and 32, a method of manufacturing a semiconductor device, further comprising: patterning the crystalline semiconductor layer to form an island shape (col. 13, lines 60-65, ***Note***: that the Examiner takes the position that patterning the crystalline semiconductor layer to form an island shape is performed since the SOI wafer, taught by Buynoski, may be further processed by methods known in the art for preparing a desired semiconductor device). Also, Buynoski shows, pertaining to claims 18, 23 and 33, a method of manufacturing a semiconductor device, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to 5 $\times 10^{18}/cm^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 7, lines 35-42).

Buynoski shows, pertaining to claim 29, a method of manufacturing a semiconductor device, comprising: forming an amorphous semiconductor layer over a substrate **12** that has an insulated surface **14** (figure 1; 4, lines 40-47; col. 13, lines 1-10 and 22-43, ***Note***: that the

Examiner takes the position that a amorphous semiconductor layer is included); adding a metal element for accelerating crystallization to the amorphous semiconductor (figure 1; 4, lines 40-47; col. 9, lines 43-50 for transitional metals, ***Note***: that the Examiner takes the position that adding a metal element for accelerating crystallization is performed, since the monocrystalline silicon film, taught by Buynoski, includes transitional metals that are conventionally used for crystallization); crystallizing the amorphous semiconductor layer by heat to obtain a crystalline semiconductor layer (figure 1; 4, lines 40-47, ***Note***: that the Examiner takes the position that a crystalline semiconductor layer is formed by heating an amorphous semiconductor layer since a monocrystalline silicon film is taught by Buynoski); introducing an impurity element **18/20** into the crystalline semiconductor layer by accelerating the impurity element with the acceleration voltage 30 kV or less (figure 2; col. 5, lines 40-46, ***Note***: that the Examiner takes the position that the acceleration voltage of 30 kV or less is incorporated since Buynoski teaches conventional ion implantation techniques); removing a surface portion of the crystalline semiconductor layer which is recrystallized (figure 5; col. 8, lines 3-8 for heat treatment; col. 10, lines 17-20, ***Note***: that the Examiner takes the position that the surface of the crystalline semiconductor layer is re-crystallized since the semiconductor wafer, taught by Buynoski, is subjected to a heat treatment for the removal of the impurities within the monocrystalline silicon film). In addition, Buynoski shows, pertaining to claim 35, a method of manufacturing a semiconductor device, wherein a thickness of the surface portion of the crystalline semiconductor layer removed is 10 nm to 50 nm (col. 13, lines 1-10 and 22-43). Also, Buynoski shows, pertaining to claim 36, a method of manufacturing a semiconductor device, further comprising: patterning the crystalline semiconductor layer to form an island shape (col. 13, lines

60-65, ***Note***: that the Examiner takes the position that patterning the crystalline semiconductor layer to form an island shape is performed since the SOI wafer, taught by Buynoski, may be further processed by methods known in the art for preparing a desired semiconductor device). Finally, Buynoski shows, pertaining to claim 37, a method of manufacturing a semiconductor device, wherein a concentration of the impurity element in the crystalline semiconductor layer is 1×10^{15} to $5 \times 10^{18}/cm^3$ and in the range of the concentration being $\pm 10\%$ for an average (col. 7, lines 35-42).

However, Buynoski fails to show, pertaining to claims 1, 3, 13, 19, 28 and 29, irradiating the crystalline semiconductor layer with laser light to redistribute the impurity (after introducing the impurity element, for claims 13, 19, 28 and 29). In addition, Buynoski fails to show, pertaining to claims 5, 7, 15, 20, 30 and 34, a method of manufacturing a semiconductor device, wherein a source of the laser light is one selected from a continuous wave, YAG laser, YVO_4 laser, YLF laser, and $YAlO_3$ laser.

Hwang teaches, in figures 1a-1g, and corresponding text, a conventional method of manufacturing a semiconductor device, where a laser irradiation technique is used for crystallization of a semiconductor layer and activation of the implanted impurity element (col. 1, lines 50-63)

It would have been obvious to one of ordinary skill in the art incorporate, irradiating the crystalline semiconductor layer with laser light to redistribute the impurity (after introducing the impurity element); wherein a source of the laser light is one selected from a continuous wave, YAG laser, YVO_4 laser, YLF laser, and $YAlO_3$ laser, in the method of Buynoski, pertaining to claims 1, 3, 5, 7, 13, 15, 19, 20, 28, 29, 30 and 34, according to the conventional teachings of

Hwang, with the motivation of activating using least one of the above conventional lasers, thereby redistributing, the impurities implanted within the crystalline semiconductor layer, for the purpose of creating active source/drain regions for a semiconductor device.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Stanetta D. Isaac whose telephone number is 571-272-1671. The examiner can normally be reached on Monday-Friday 9:30am -6:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Lebentritt can be reached on 571-272-1873. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Stanetta Isaac
Patent Examiner
March 17, 2005

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